

## REMARKS/ARGUMENTS

In the Final Office action mailed May 7, 2009, claims 1, 3, 4, and 6 – 9 were rejected. In response, Applicant has amended claim 1, canceled claims 6 and 7, and added new claims 10 – 12. Applicant submits herewith a Request for Continued Examination (RCE). Applicant hereby requests reconsideration of the application in view of the amended claim, the added claim, RCE, and the below provided remarks.

### Claim Rejections

Claims 1, 3, 4, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (U.S. Pat. No. 5,384,570) in view of Applicant's Admitted Prior Art (AAPA), Fig. 2. Claim 1 has been amended recite two dummy switches and to particularly point out that the two bootstrap switches (14a and 14b) are connected to the same level shifted output version of the output signal (Vs). Support for the amendments to claim 1 are found in Applicant's specification at, for example, claims 6 and 7, paragraphs [0021] and [0022] (U.S. Pub. No. 2006/0192546 A1), and Fig. 5.

As amended, claim 1 recites:

“A single track-and-hold circuit having an input signal (Vin) and an output signal (Vs), a bootstrap switch (14a) having as its inputs a clock signal (clk) and an input signal (vin), said input signal (vin) of said bootstrap switch (14a) being connected to said output signal (Vs) of said circuit via a current source (20) and a buffering transistor (30), characterized in that said input signal (vin) of said bootstrap switch (14a) comprises said output signal (Vs) of said circuit; said single track-and-hold circuit further comprising a capacitor (12), said input signal (Vin) being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal (clkboot) equal to said input signal (Vin) added to a supply voltage (Vdd);

including a second bootstrap switch (14b), the input signal (vin) of which is connected to said output signal (Vs) of said single track-and-hold circuit via said current source (20) and said buffering transistor (30) of said single track-and-hold circuit; and

two dummy switches (16) connected on either side of said switch (10) and clocked in anti-phase to said switch (10) by anti-phase boot clock signal (clknboot);

wherein both said bootstrap switch (14a) and said bootstrap switch (14b) are connected to the same level shifted output signal (Vs).

” (emphasis added)

As recited in amended claim 1, the first and second bootstrap switches are connected to the same level shifted version of the output signal (Vs). That is, the first and second bootstrap switches are connected to the output signal (Vs) via the same current source (20) and the same buffering transistor (30).

Applicant asserts that a *prima facie* case of obviousness has not been established with respect to claim 1 because Dedic in view of the AAPA do not teach all of the limitations related to the second bootstrap switch (14b).

The Final Office action addresses the limitations of bootstrap switch (14a) as follows:

“AAPA in Fig. 3 teaches...a bootstrap switch (14a) having as its inputs a clock signal and an input signal (vin);” (emphasis added)

“The combined teachings of Dedic and AAPA further teach said input signal (AAPA, Fig. 3, vin) of said bootstrap switch (AAPA, Fig. 3, 14a) being connected to said output signal (Dedic, Vo) of said circuit via a current source (Dedic, 32) and a buffering transistor (Dedic, 33) characterized in that said input signal (AAPA, Fig. 3 vin) of said bootstrap switch (AAPA, Fig. 3, 14a) comprises said output signal (Dedic, Vo) of said circuit;” (emphasis added) (Final Office action, page 3)

The Final Office action appears to state that the second bootstrap switch (14b) is taught by AAPA in Fig. 3. The Final Office action addresses the limitations of bootstrap switch (14b) as follows:

“including a second bootstrap switch (14b).” (Final Office action, page 3)

With respect to Fig. 3 of the AAPA, Applicant points out that Fig. 3 teaches first and second bootstrap switches (14a and 14b), however, neither of the two bootstrap switches have an input signal that is connected to the output signal. In particular, the input (Vin) to the bootstrap switches (14a and 14b) of Fig. 3 is not connected to the output signal (V).

Additionally, Applicant asserts that Dedic does not teach an output signal connected to a second bootstrap switch as recited in amended claim 1. While Dedic may teach an output signal connected to one bootstrap switch (see Dedic, Fig. 3), Dedic does not teach or suggest that the same output signal is connected to two bootstrap switches as recited in amended claim 1.

Because neither the AAPA nor Dedic teach a level shifted version of the output signal (Vs) connected to a second bootstrap switch as recited in amended claim

1, Applicant asserts that amended claim 1 is patentable over Dedic in view of the AAPA.

Dependent Claims 3, 4, 8, and 9

Claims 3, 4, 8, and 9 are dependent on claim 1. Applicant respectfully asserts claims 3, 4, 8, and 9 are allowable at least based on an allowable base claim.

New claims 10 – 12

New claim 10 recites in part that “Vgs of switch (10) is equal to Vdd + Vlevelshift.” Support for new claim 10 is found in Applicant’s specification at, for example, paragraph [0021].

New claim 11 recites in part that “Vgs of switch (10) is equal to Vdd + 0.5V.” Support for new claim 10 is found in Applicant’s specification at, for example, paragraph [0021].

New claim 12 recites in part that “said output signal (Vs) is constant in hold mode so there is no crosstalk to said capacitor (12).” Support for new claim 10 is found in Applicant’s specification at, for example, paragraph [0022].

## CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

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Mark A. Wilson  
Reg. No. 43,994

Wilson & Ham  
PMB: 348  
2530 Berryessa Road  
San Jose, CA 95132  
Phone: (925) 249-1300  
Fax: (925) 249-0111